

**AMENDMENT(S) TO THE SPECIFICATION**

**Please replace the paragraph [0007] beginning at page 2, line 20, with the following rewritten paragraph:**

[0007] Then, in an effort to increase the simplicity and flexibility of on-board power distribution design, fully regulated converters were used to generate intermediate bus voltages, which were then converted to point-of-load voltages via point-of-load power converters (POLs). For example, in one scheme (not shown), a -48Vin nominal input is converted into a 3.3 volt intermediate bus voltage using a single isolate isolated converter. This intermediate bus voltage is supplied directly to the most power-hungry loads on the board, while less power-hungry loads receive power via respective POL converters. ~~In another scheme, as illustrated in Figure 2; nominal -48V is converted into a 12V intermediate bus voltage 205 via a single isolated converter 210. The intermediate bus voltage 205 is then converted to various point-of-load voltages via respective POLs 215a, 215b, 215c . . . , 215n. In order to maximize throughput efficiency and minimize cost of either two-stage scheme, each power conversion stage must be carefully optimized. However, throughput efficiency of these schemes is typically lower when compared to power distribution designs employing multiple isolated converters low.~~

**Please replace the paragraph [0008] beginning at page 3, line 5, with the following rewritten paragraph:**

[0008] It is an object of the present invention to overcome the disadvantages of conventional two-stage power distribution schemes by providing a cost and space efficient power distribution design that employs less components, while at the same time satisfying the ever increasing power demands of many of today's applications. For this purpose, an exemplary embodiment of the present invention takes advantage of the fact that it is not necessary for the isolated converter to precisely control the intermediate bus voltage when using tightly regulated POL converters. Rather, effective performance can be achieved by running the converter open-loop in an unregulated ~~regulated~~ fashion.

Please replace the paragraph [0012] beginning at page 4, line 9, with the following rewritten paragraph:

[0012] Figure 2 is a block diagram showing ~~another conventional~~ a basic two-stage power conversion architecture according to the present invention.

After the section heading "DETAILED DESCRIPTION" at 5, line 1, please add the following new paragraph:

In a basic scheme according to an embodiment of the invention, as illustrated in Figure 2, nominal -48V is converted into a 12V intermediate bus voltage 205 via a single isolated converter 210. The intermediate bus voltage 205 is then converted to various point-of-load voltages via respective POLs 215a, 215b, 215c . . . 215n.